SIPEARL

How to design and deploy a European high-performance microprocessor?

It will help solve sovereign strategic scientific societal
and environmental challenges with a reduced carbon footprint

26 April 2024 – FRnOG #39

SiPearl in a nutshell

Building the European high-performance low-power microprocessor

Incorporated
In June 2019

Financing
Series-A (to date): €113m

Funded
By the European Union

Key partnerships
Joint-offering with

Arm architecture
Energy-efficiency quick time to market, proven ecosystem

Identified customers
Server manufacturers based on user specifications: First, EuroHPC ecosystem before going global.

+190

Employees

from

6 locations
Maisons-Laffitte (HQ), Barcelona, Duisburg, Grenoble, Massy, Sophia Antipolis

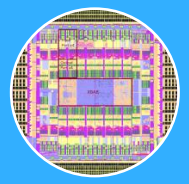
Development flow

Project Kick-off → Linux Boot on full model → Tape-out → Engineering sample → General Availibility

Architecture & Micro-Architecture

RTL Design & Integration & DFT

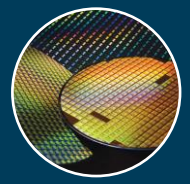
Verification (RTL Simulation)



Physical Design

Prototypes Manufacturing (TSMC)

Bring-up/ Validation

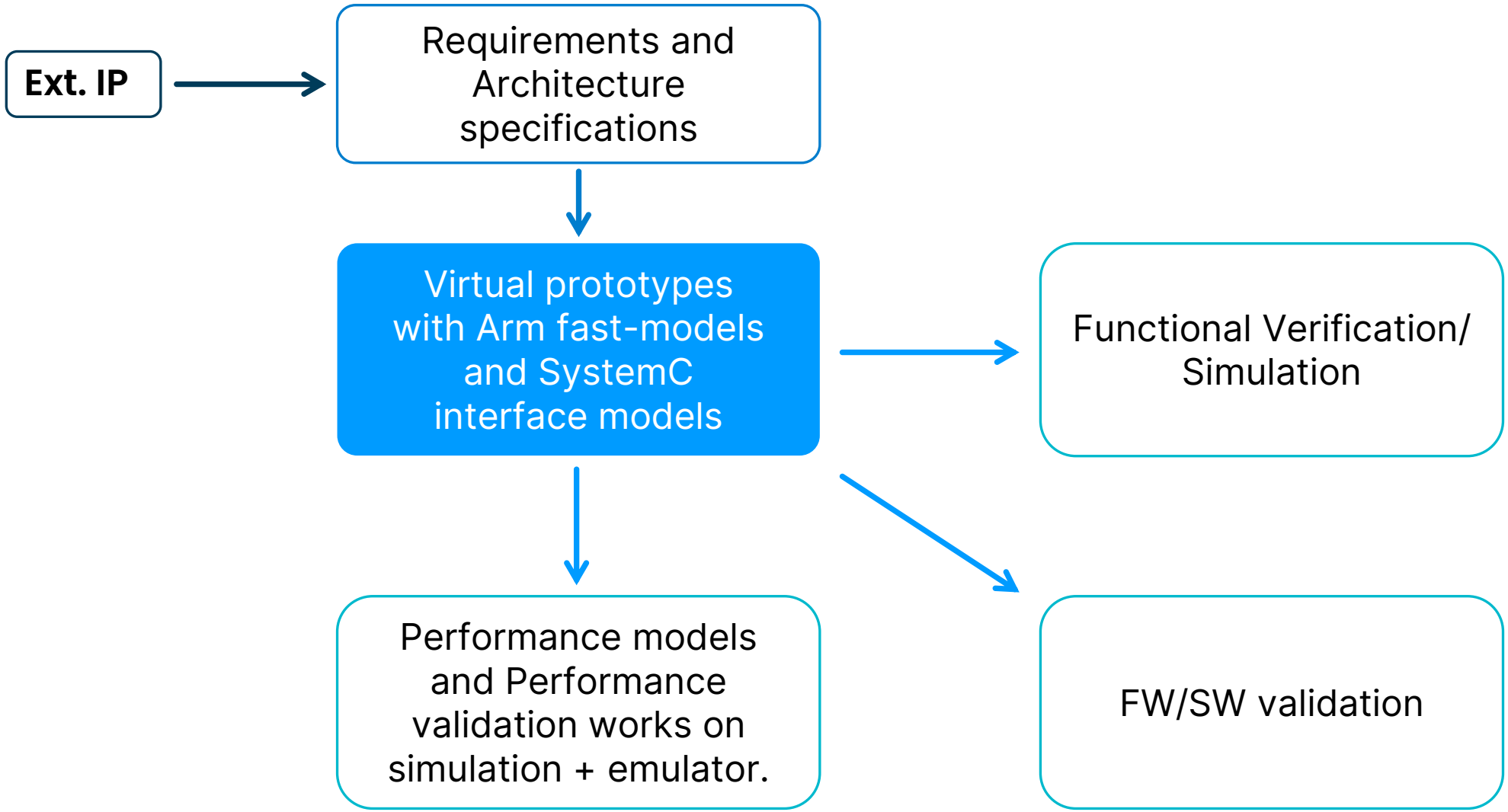


Production (TSMC)

Fast models & Virtual prototyping

Software

Virtual Prototype: Key component of our verification strategy



Software test strategy

Different types of tests are planned to cover System and SW requirements

- Unit tests are done for new developments (mainly at FW level, for some in-house drivers)
- Integration tests are done to check that all SW components are working together (one of this test is booting a full Linux on the targeted platform)
- System tests are more covering advanced SW features (like BMC-SOC communication)

All the tests are developed to be usable on different types of platforms

- Virtual prototyping
- Emulation or Hybrid platforms (including some FPGA boards connected to BMC platforms)
- Silicon bring-up

Tests execution is part of our CI/CD strategy

- Each test execution is automated to ease regression tests
- Selection of test is assessed for each platform based on the platform constraints (Emulation is slow so HP application performances tests are not done)

Test coverage is done by importing all the results in our Requirements / Test management system (Polarion)

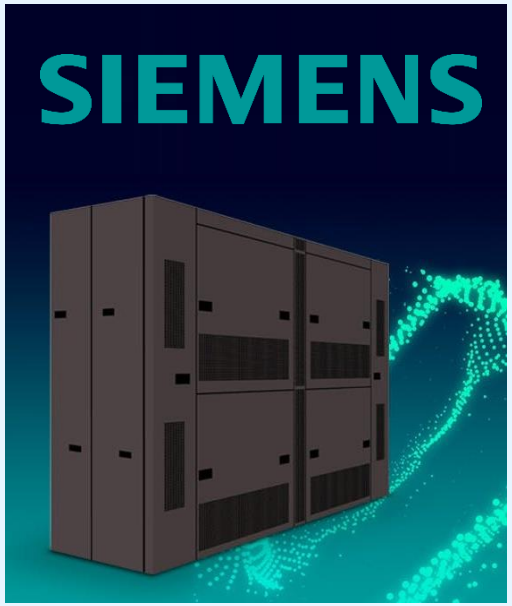
- All tests are described in associated tests plans
- Tests plans are reviewed by peers and architects

Software and System validation targets

Tests	Target
UEFI self certification tests (UEFI-SCT)	VP / Emulation / Silicon
Firmware Test Suite (FWTS)	VP / Emulation / Silicon
Server Base System Architecture test suite (SBSA)	VP / Emulation / Silicon
Micro kernels	Simulation / Emulation
Mini-Apps	VP* / Emulation / Silicon
Benchmarks / Application	VP* / Emulation* / Silicon
Compiler / Libraries / Tools tuning	VP* / Emulation* / Silicon
Performance validation	Emulation* / Silicon

** Limited scope depending on performance*

Veloce Strato



Veloce
at its full capacity

100% of capacity in full ownership

2 Veloce with
2x64 new generation cards

Veloce control servers

Investment to date: €15m
x2 in 2024

Rhea1, our 1st generation microprocessor

Designed with high-performance energy-efficient Arm Neoverse V1 platform

High performance per watt: Arm, global leader in the smartphone business

- Arm ISA power efficiency

Very high memory bandwidth

Built-in HBM

- Ideal performances for Generative AI inference
- >1Tbyte/s in terms of throuput

Unique memory architecture

- High Byte/Flop
- 2 first patents

Openess

- Arm ecosystem from IoT/edge to HPC and cloud
- Common platform – chiplet-based ecosystem

Fully auditable – backdoor-free

Pre-integration with proven accelerator

- AMD, Intel, Graphcore, Nvidia
- More to come with quantum computing and new accelerators

Rhea1 will deliver extraordinary compute performance and efficiency with an unmatched Byte/Flop ratio.

SiPearl corporate vision and strategy

A range of HPC & AI inference microprocessors with a reduced environmental footprint to conquer the European market and beyond

HPC & AI inference

SiPearl entry business: European HPC & AI

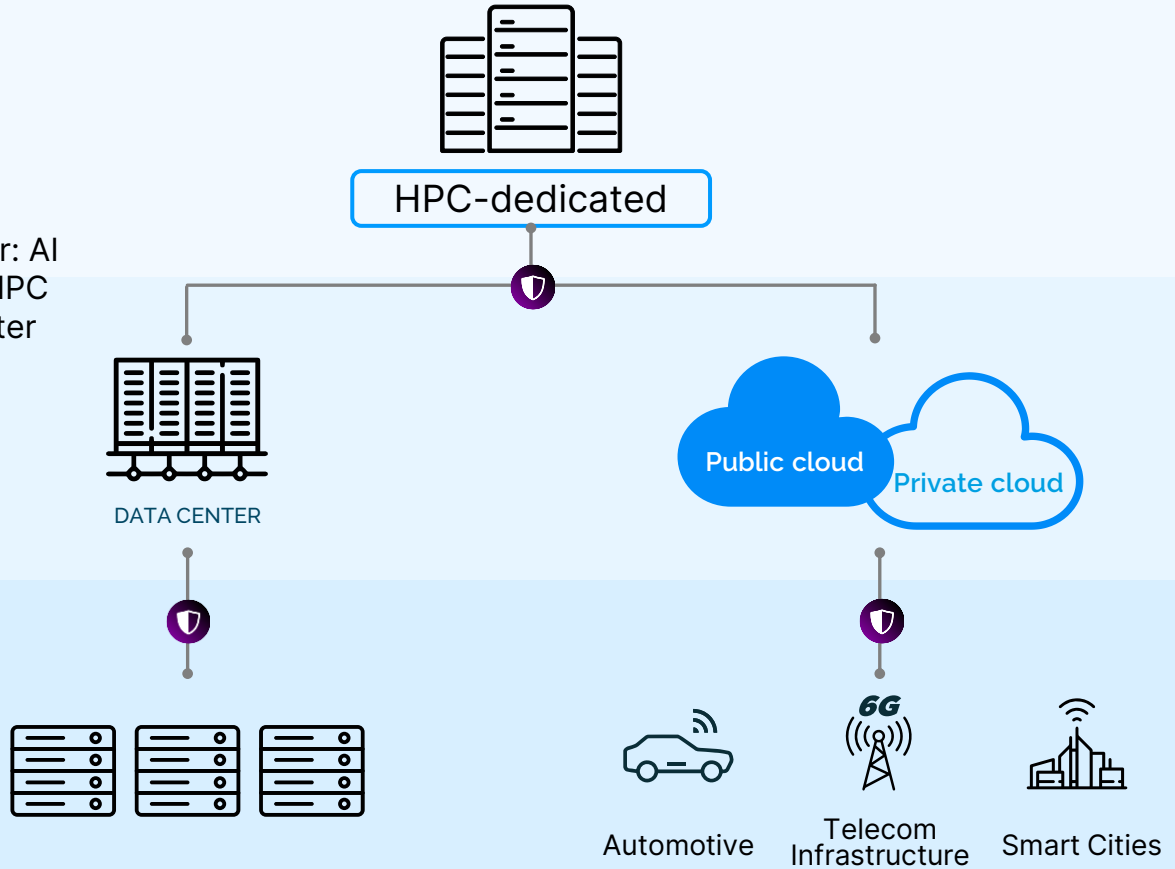
Growth vector: AI Inference in HPC and Data center

Data center-Central

Data centers, private and public cloud

Data center-Edge

Small Compute Farms around 6G infrastructure



About... SiPearl

SiPearl is building the European high-performance low-power microprocessor dedicated to supercomputing and AI inference. This new generation of microprocessors will first target EuroHPC Joint Undertaking ecosystem, which is deploying world-class supercomputing infrastructures in Europe for solving strategic sovereign challenges in medical research, security, energy management and climate with a reduced environmental footprint.

SiPearl is working in close collaboration with its 30 partners from the European Processor Initiative (EPI) consortium - leading names from the scientific community, supercomputing centres and industry - which are its stakeholders, future clients and end-users.

SiPearl employs more than 190 people in France (Maisons-Laffitte, Grenoble, Massy, Sophia Antipolis), Germany (Duisburg) and Spain (Barcelona).

Contact

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Funded by
the European Union

European Processor Initiative
epi