Software friendly solution for new Levels of Supercomputing

VSORA Software Development Flow

SORA

We have **built a technological** edge early on that positions us to disrupt the AI computation environment.

Inception 2015 Market release for Autonomous driving

2018

Step 1: Build the tech Early on we saw the memory wall bottleneck on AI computation Step 2: Field test the tech

Autonomous driving was the most demanding market, we tackled it *Customer interactions: Germany,*

USA, Japan



Embraced Generative Al wave

2022

Step 3: Deploy the tech

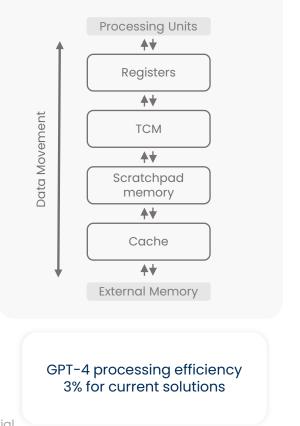
Our technology ideally positions us to disrupt current chip offering and massively benefit from the exponential growth in GenAl applications

Processing power

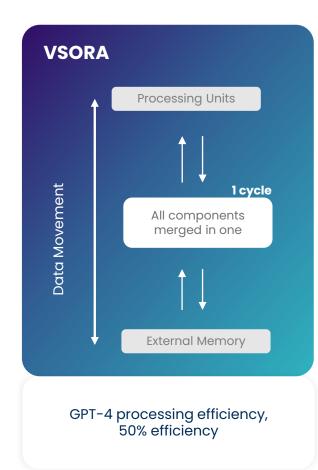
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New architecture to Break the Memory Wall!

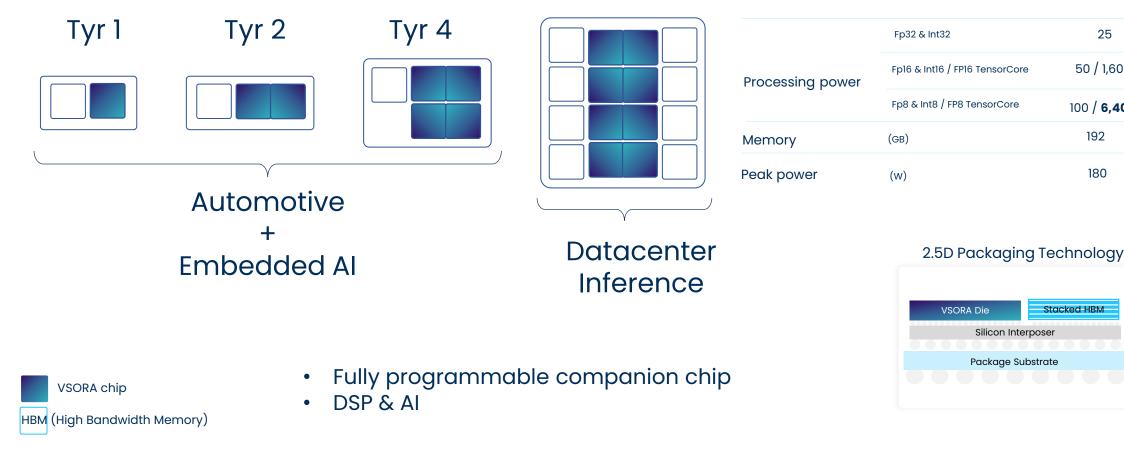
Scalar native architecture



Vectors/Matrices native architecture



VSORA Product Lines Embedded AI + Datacenter



Jotunn8

Strictly confidential

25

50 / 1,600*

100 / 6,400*

192

180

VSORA

ΑΙ

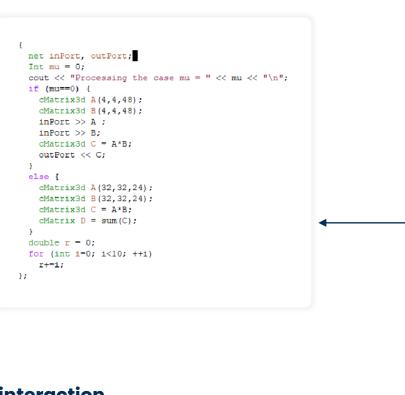
Quick & Simple SW development flow

High-level coding

Matlab-like / Tensorflow-like / C++ No need for low-level programming!

Common code for algorithms & main processor

Jotunn functional co-processor to main processor Physical code execution location transparent to user Code separated by compiler at compilation



USORA Graph

Tensorflow, Pytorch, ONNX,...

System code Matlab-like / Tensorflow-like / C++



Main Processoi AI & DSP

Multiple simulation platforms

Better interaction between teams

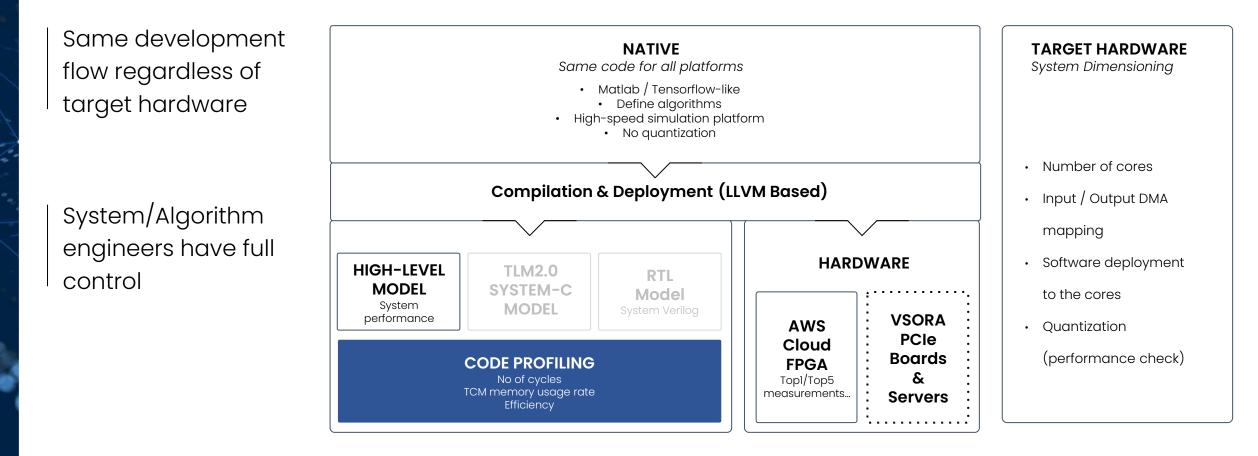
Lower risk

Faster TTM

Higher flexibility

Strictly confidential

System deployment and Simulation Platforms Core Chip / Software / System



Thank you